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(56) Documents Cited
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(54) Micromechanical structures

(57) The micromechanical structures (16) produced in a separate wafer (14) and this wafer (14) is aligned with and placed on a wafer (12) containing integrated circuits by interposing a metallic connecting element (20). The device may be used as a capacitive acceleration sensor.

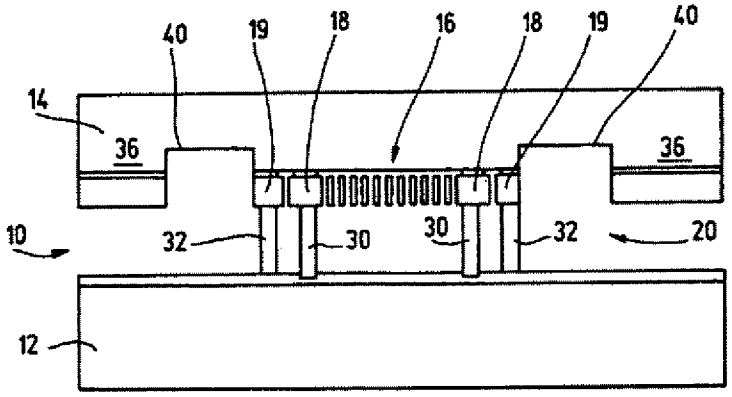

Fig. 2

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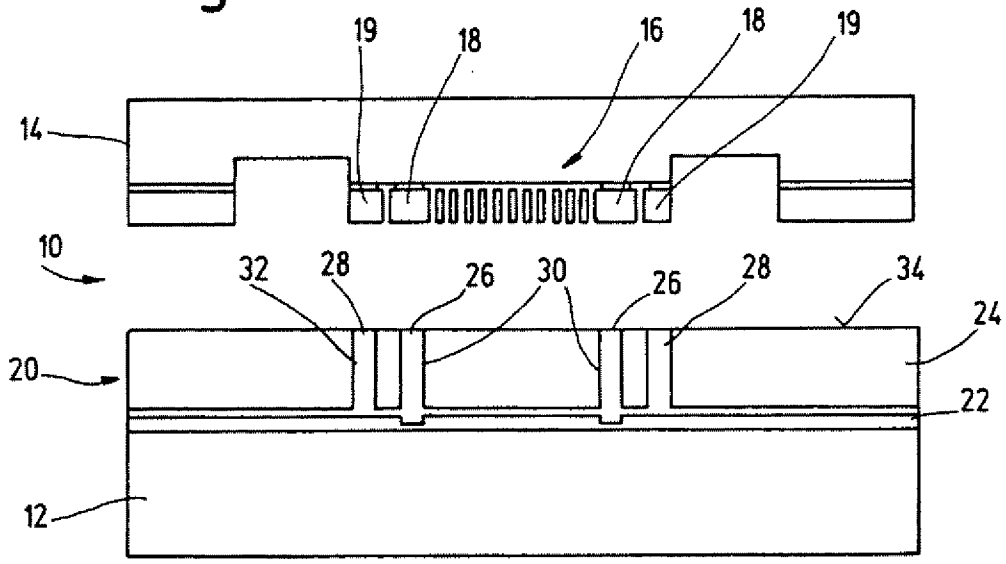
Fig. 1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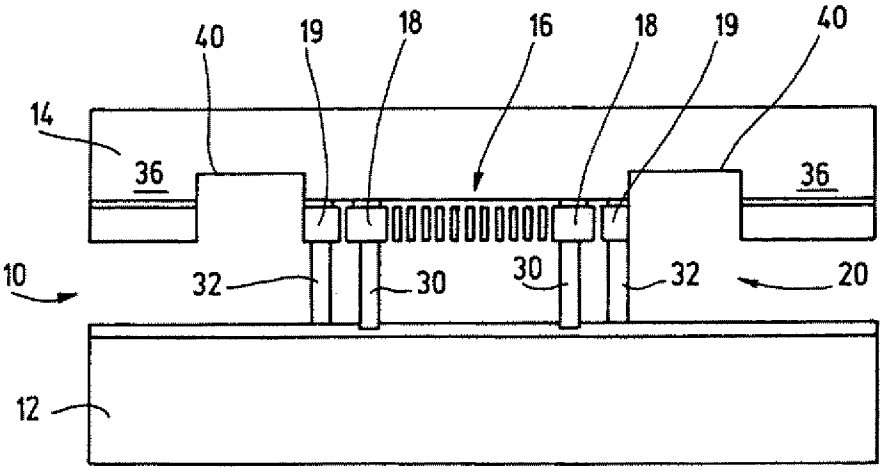
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Fig. 2

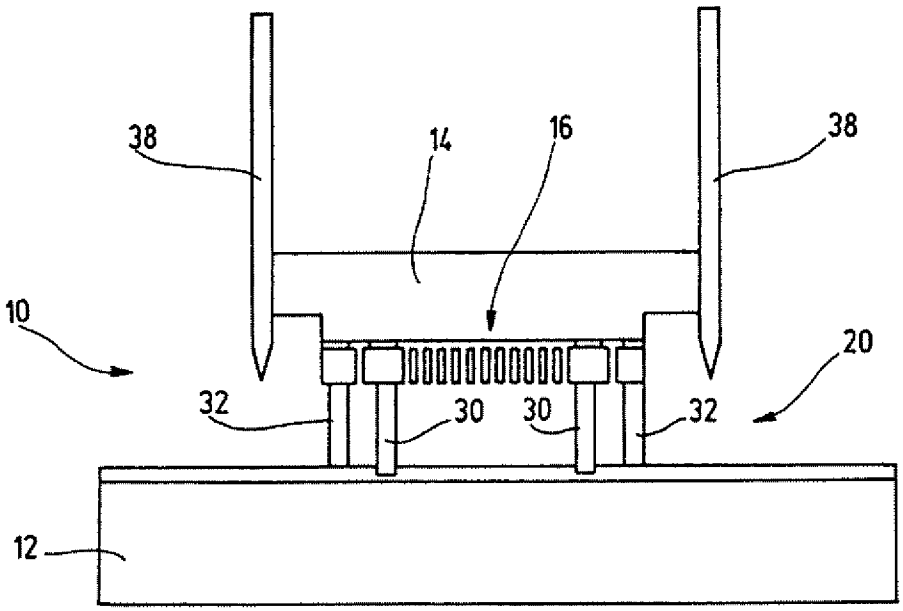

Fig. 3

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Process for the manufacture of semiconductor components containing micromechanical structures

The invention concerns a process for the manufacture of semiconductor components containing micromechanical structures according to the preamble of Claim 1.

Prior art

It is known that micromechanical structures can be placed on the surface of semiconductor components, for example on the surface of silicon wafers containing integrated circuits (ICs). These can, for example, be freely movable sensor elements constructed as capacitive acceleration sensors consisting of a spring-suspended seismic mass and a comb structure arrangement for the capacitive evaluation of the deflection of the seismic mass due to acceleration.

For example, to obtain such components, the traditional processes for producing micromechanical surface structures employ sacrificial layers integrated into the wafer structure, and active silicon layers above them, for example polysilicon on silicon oxide islands, necessitating major intervention in the IC process.

According to another known manufacturing process, these sensor elements are produced in electro-deposited metal layers with the aid of the LIGA technique. In the LIGA process, structures with high X-ray resistance are

electrically shaped by synchrotron radiation to obtain a first forming die. This forming die is then used to stamp under high pressure polymer layers deposited on wafers, thus resulting in a negative mould which is then electrically backfilled. The polymer mould is subsequently destroyed, thus exposing the sensor element. The disadvantage here is that synchrotron radiation can only be implemented with a high degree of complexity, and thus high cost, by means of additional synchrotron equipment which is not the usual equipment for semiconductor component manufacture. Moreover, due to the high die pressures during the stamping out of the negative structures there is a risk of damaging the wafer, the forming die or the electronic circuits integrated into the wafer. Furthermore, precise alignment of the sensor elements with the circuits contained on the wafer is difficult during stamping. Due to wear in the forming die it is necessary to create several daughter moulds by reverse stamping before the actual manufacture of the sensor elements can take place. Until now the function of the process as a whole could not be proven in practice. The stamping on the IC wafer always represented a risky intervention in the IC process.

A process in which the micromechanical structures are constructed at a later stage on a fully processed semiconductor component by forming the subsequent structures in additionally deposited layers and grown by electro-deposition later, is disclosed by DE 44 18 163 A1. The disadvantage here is that due to the electro-deposition of the micromechanical structures, the entire semiconductor component consists of different materials, which, due its different thermal characteristics, can lead to failures at the limits of the application of the semiconductor components.

Advantages of the invention

The process according to the invention, with the features stated in Claim 1, offers the advantage that a compact semiconductor component having integrated micromechanical structures can be created in a simple manner. By producing the micromechanical structures in a separate wafer and aligning this wafer with and placing it on the wafer containing the integrated circuits by interposing at least one electrical and mechanical connecting element, and without intervening in the manufacturing process of the integrated circuits, it is advantageously possible to produce the additional wafer containing the micromechanical structures and combine an electrical coupling and mechanical housing for the micromechanical structures with the joining of the two wafers. Due to the arrangement of the micromechanical structures on the wafer containing the integrated circuits no additional space is required on the wafer containing the integrated circuits. The simultaneous hermetic encapsulation of the micromechanical structures is very advantageous since these are consequently reliably packaged against all kinds of environmental influences.

Advantageous developments of the invention are revealed by the features stated in the sub-claims.

Drawings

The invention is explained in further detail below in an exemplary embodiment with the aid of the associated drawings. The individual process steps for the manufacture of a semiconductor component containing micromechanical structures are clearly shown in Figures 1 to 3.

Description of the exemplary embodiment

The main parts of a semiconductor component 10 are shown in their initial state in a schematic sectional representation in Figure 1. The semiconductor component 10 consists of a first wafer 12, for example a silicon wafer, that can contain integrated circuits, not illustrated here. A second wafer 14 that has micromechanical structures, generally denoted here by 16, is assigned to the first wafer 12. It is not intended to go into the details of the production of the micromechanical structures 16 in this present description. Spring-suspended seismic masses and comb structures for driving the seismic masses or for sensing a displacement of the seismic masses due to acceleration can be provided as micromechanical structures 16. The second wafer 14 is for example likewise a silicon wafer having a layer structure that is suitable for the production of the micromechanical structures 14. This layer structure can, for example, consist of a silicon-on-insulator material, epitaxially reinforced polysilicon, on an intermediate oxide with subsequent surface polish. The production of the micromechanical structures 16 is effected, for example, by means of known process steps of a combination of anisotropic plasma etching and isotropic undercutting. During the manufacture of the micromechanical structures 16, relatively large-area contact regions 18 and 19 for applying signals to or tapping signals from the micromechanical structures 16 are assigned to said micromechanical structures.

At least one electrical and mechanical connecting element 20, whose manufacture is explained in detail below, is arranged between the wafers 12 and 14, that is to say between the electronic part and the sensor part of the semiconductor component 10.

The surface of the fully processed wafer 12 is provided with a metal structure 22. A continuous, flat metallic coating,

for example a sputtered chromium/copper alloy, can be applied to the wafer 12 for this purpose. A relatively thick photoresist layer 24 is applied to the metal structure 22 by spin-coating, for example. First structures 26 and a second structure 28 are placed within the photoresist layer 24 by means of known photolithographic processes. For this, a mask, not shown, is placed on the photoresist layer 24 and resist material is dissolved or etched away in the subsequent structures 26 and 28. The structures 26 are arranged so that these are geometrically allocated on the one hand to the contact pads provided on the wafer 12 for electrical connection to the micromechanical structures 16 and on the other hand to the contact regions 18 of the micromechanical structures 16. The structure 28 produces a channel which when viewed from above encloses the structures 26, the geometry of the area enclosed by the structure corresponding to the size of the micromechanical structures 16.

In a following process step, the structures 26 and 28 in the photoresist layer 24 are backfilled metallically by means of an electro-deposition process, for example. This results in metallic regions 30 in the structures 26, which pass through the photoresist layer 24, and a metallic region 32 in the structure 28, which encloses the metallic regions 30 more or less in the form of a trough.

After metallic-deposition, the surface 34 can be levelled and smoothed by a suitable method, for example by mechanical polishing. A completely flat surface is thus obtained on the sides of the metallic regions 30 and 32, respectively, facing away from the wafer 12. During this smoothing process the wafer 12 containing the integrated circuits is protected by the photoresist layer 24, so that damage to the wafer 12 can be eliminated.

In a following process step the photoresist layer 24 is now removed, for example incinerated in the oxygen plasma in a generally known manner. The metal structure 22 is then selectively removed, for example etched away, on the surface of the wafer 12 and between the high metallic regions 30 and 32.

In a following step, the subsequent contact areas between the metallic regions 30 and 32 of the connecting element 20 and the contact regions 18 and 19, respectively, of the wafer 14 undergo suitable chemical pretreatment, for example hydrophilic treatment. Due to Van-der-Waals forces, this results in a permanent contact between the contact regions 18 and 19, comprised of silicon, and the metallic regions 30 and 32, respectively. It is also possible to employ a solderable metal or to electroplate or print a thin solder layer.

The wafers 12 and 14 are then aligned and brought into contact, that is to say these are arranged one above the other so that the metallic regions 30 come into contact with the contact regions 18. Because the contact regions 18 were applied over a relative large area, the intended joining of the wafers 12 and 14 can be effected with adequately high alignment accuracy, without necessitating a highly-precise and complex alignment. As a result, the metallic regions 32 make simultaneous contact with the contact regions 19.

A permanent connection is then made between the metallic regions 30 and 32, and the contact regions 18 and 19, respectively. To do this, the wafer 14 can be briefly heated, while the wafer 12 is cooled, for example. This process step can be carried out by means of a suitable device, which has, for example, a cooling device in contact with the wafer 12 and a heating device in contact with the wafer 14. The result of this is that the contact points between the metallic regions 30 and 32, and the contact

regions 18 and 19, respectively, can be heated up to temperatures above 450 °C, while the wafer 12 and the integrated circuits arranged thereon are protected against excessive heating. The heating up of the contact regions results in the formation of an alloy between the silicon of the contact regions 18 and 19 and the metal of the metallic regions 30 and 32, thus producing a permanent mechanical and electrically-conducting connection between the wafers 12 and 14 via the connecting element 20. This can be further reinforced by a solder layer applied in advance.

According to further exemplary embodiments, instead of producing the alloy, a connection can be made between the contact regions 18 and 19, and the metallic regions 30 and 32, respectively, by other techniques, for example the use of conductive adhesives or solder.

For signal conduction, after the wafers 12 and 14 have been joined, an electrical connection is made via the metallic regions 30 between the integrated circuits in the wafer 12 and the micromechanical structures 16 in the wafer 14. The metallic regions 32 enclosing the micromechanical structures 16 in the form of a wall on the one hand increase the stability of the mechanical connection between the wafers 12 and 14 and on the other hand provide a hermetic encapsulation of the micromechanical structures 16. The micromechanical structures 16 are completely encapsulated in this way by the wafer 14 and the wafer 12, respectively, and the metallic region 32, so that environmental influences can have no effect on the operational capability of the sensitive micromechanical structures 16. Moreover, this complete encapsulation reliably prevents damage to the micromechanical structures during further process steps, such as for example separation of the components 10 and subsequent enclosure, for example plastic encapsulation.

In a following process step, illustrated in Figure 3, the surface of the wafer 12 is further exposed by removing the superfluous sections 36 of the wafer 14, that is to say those sections enclosing the micromechanical structure 16, that are not required for the further operation of the semiconductor component 10. The sections 36 can be simply removed by means of a saw cut 38 shown here. This saw cut can be made, for example, by mechanical means or suitable laser techniques etc. To ensure that no damage occurs to the wafer 12 during this separation of the sections 36, trough-type recesses 40 which define the desired separation points can be provided during the manufacture of the wafer 14.

Alternatively, prior to the bonding of the wafer 14 to the wafer 12 it is also possible to separate the micromechanical structures 16 from a composite wafer in advance, so that the process step illustrated in Figure 3 would be eliminated in an already assembled semiconductor component 10.

Alternatively, prior to the bonding of the wafer 14 to the wafer 12 it is also possible to separate the IC chips of the wafer 12 and bond them to the sensor chips of the still complete sensor wafer 14. The sensors are then separated; this is advantageous when the IC wafer already has a difficult, that is to say a very uneven topography due to the numerous semiconductor process steps, and would be difficult to bond over the whole area.

By and large it is possible to manufacture semiconductor components 10 with integrated micromechanical structures 16 in which only one additional masking level is necessary to produce the connecting element 20 which provides the electrical and mechanical coupling. This additional masking level can be applied after completion of all the processing steps of the wafer 12, thus eliminating intervention in the processing of the integrated circuits.

The finished semiconductor component 10 provides a further advantage, since both the wafer 12 and the wafer 14 consist of the same silicon material which has an identical thermal characteristic with a continuous load or a change of load, so that the thermal effect on the long-term life span of the semiconductor component 10 can be minimized.

Claims

1. Process for the manufacture of semiconductor components containing micromechanical structures, **characterised in that** the micromechanical structures (16) are produced in a separate wafer (14) and this wafer is aligned with and placed on a wafer (12) containing the integrated circuits by interposing a connecting element (20).

2. Process according to Claim 1, **characterised in that** the connecting element (20) is placed on the surface of the fully processed wafer (12).

3. Process according to Claim 2, **characterised in that** the wafer (12) is provided with a metal structure (layer) (22), onto which a photoresist layer (24) is then applied.

4. Process according to one of the preceding Claims, **characterised in that** openings for producing structures (26, 28) are placed in the photoresist layer (24) and are used for the subsequent electrical and mechanical connection of the wafers (12, 14).

5. Process according to one of the preceding Claims, **characterised in that** the openings (26, 28) are backfilled to form metallic structures (30, 32), the photoresist layer (24) and the metal structure (22) are removed so that only relatively high metallic regions (30, 32) form the connecting part (20).

6. Process according to one of the preceding Claims, **characterised in that** the metallic regions (30) provide an electrical connection between the integrated circuit of the wafer (12) and the micromechanical structures (16) of the wafer (14).

7. Process according to one of the preceding Claims, **characterised in that** the metallic regions (32) completely enclose the metallic regions (30) in the form of a ring.

8. Process according to one of the preceding Claims, **characterised in that** the wafers (12, 14) are joined by bringing contact regions (18, 19) of the wafer (14) into contact with the metallic regions (30, 32).

9. Process according to Claim 8, **characterised in that** an intimate electrically-conducting connection is established between the contact regions (18, 19) and the metallic regions (30, 32).

10. Process according to Claim 9, **characterised in that** an alloy is produced in the contact area between the materials of the contact regions (18, 19) and the regions (30, 32) by simultaneously heating the wafer (14) and cooling the wafer (12).

11. Process according to one of the preceding Claims, **characterised in that** sections (36) of the wafer (14) not required for operation are preferably removed at previously structured reference separation points (40).

12. Semiconductor component with micromechanical structures arranged on the surface of a wafer containing integrated circuits, **characterised in that** the semiconductor component (10) is manufactured according to at least one of Claims 1 to 11.

13. A process for the manufacture of semiconductor components substantially as hereinbefore described with reference to the accompanying drawings.

14. A semiconductor component substantially as hereinbefore described with reference to the accompanying drawings.

The Patent Office

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Application No: GB 9708043.6
Claims searched: 1-14

Examiner: SJ Morgan
Date of search: 4 July 1997

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

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G1N(NAGB3,NAGB4,NAGB8,NAGBR,NAGD3,NAGD4,NAGD8,
NAGDR)

Int Cl (Ed.6): H01L; G01L; G01P

Other: Online:WPI, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A,P	US 5 572 057 (NIPPONDENSO)	
A,P	US 5 567 880 (HITACHI)	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.